## ABSTRACT OF THE DISCLOSURE

The present invention facilitates clock and data recovery for serial data streams by selecting a clock phase for each input data transition and generating a recovered clock. In order to identify data transitions, the received serial data stream is sampled N times per ideal bit time, where the minimum value for N must be greater than 2 / (1 - (2 * jitter_ratio)) and jitter_ratio is the fractional representation of the portion of the ideal bit time during which transitions can be expected or estimated to occur. On identifying a transition, a toggle phase is set. In order to avoid stale clock phase selection resulting from jitter and the like, one phase after the toggle phase is blocked or prevented from being selected for the clock. Finally, a clock phase is selected N/2 phases from the toggle phase and a recovered clock is generated by combining the individually selected clock phases.